DESIGN OF DIFFERENTIAL VOLTAGE CURRENT CONVEYOR BASED OPERATIONAL TRANSCONDUCTANCE AMPLIFIER AND ITS APPLICATION

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Abstract: In this paper, implementation a new CMOS of differential voltage current conveyor DVCC based operational transconductance amplifier with a wide linear range. The differential voltage current conveyor is used to realize a multiple input single output filter with band pass and low pass characteristics. PSPICE simulations of the proposed differential voltage current conveyor and its based filter are given using 0.18μm CMOS technology from TMSC MOSIS and dual supply voltages ±0.6V.

Keywords: Bulk-Driven transistors, differential voltage current conveyor amplifier DVCC, low-pass filter, band-pass filter, PSPICE simulation.

1. INTRODUCTION

Since its first introduction, by A. Sedra and K. Smith in 1970 [1], the second-generation current conveyor (CCII) has proved to be a versatile analog building block that can be used to implement numerous high frequency analog signal applications, like filters [2-5] and current-mode oscillators. However, when it comes to applications demanding differential or floating inputs like impedance converter circuits and current mode instrumentation amplifiers, which also require two high input impedance terminals, a single CCII block is no more sufficient. In addition, most of these applications employ floating elements in order to minimize the number of used CCII blocks. For this reason and in order to provide two high input impedance terminals, two active building blocks, namely, the differential voltage current conveyor (DVCC) and the differential difference current conveyor (DDCC) have been proposed [6]. Although both building blocks have been used in a variety of applications [7-9], their CMOS circuit realizations exhibited mainly low input and output dynamic ranges.

2. DIFFERENTIAL VOLTAGE CURRENT CONVEYOR (DVCC)

The DVCC is a five-port building block and its implementation by Diamond Transistors (DT) is shown in Fig. 1 [10].

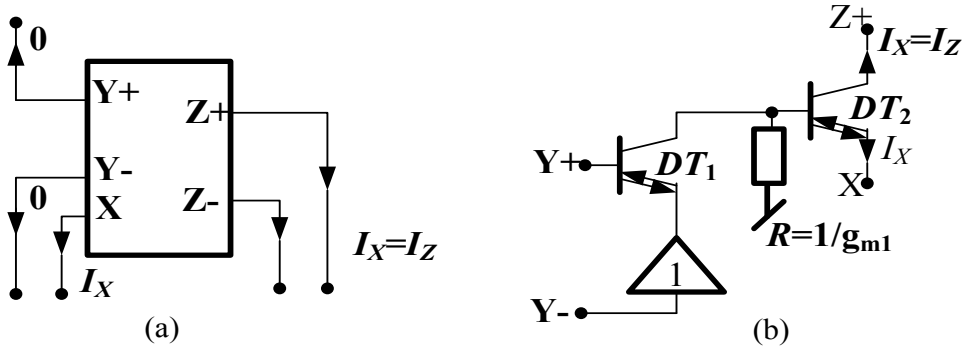

Fig. 1: (a) DVCCII+ model, (b) DVCII+ using diamond transistors and buffer.

It has two voltage input terminals: Y_+ and Y_-, which have high input impedance. The terminal X is a low impedance current input terminal. There are two high impedance current output terminals: Z_+ and Z_-. Its input-output terminal relations are given by the following matrix equation:

$$\begin{pmatrix} V_X \\ I_{Y+} \\ I_{Y-} \\ I_{Z+} \\ I_{Z-} \end{pmatrix} = \begin{pmatrix} 0 & 1 & -1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 \\ -1 & 0 & 0 & 0 & 0 \end{pmatrix} \begin{pmatrix} I_X \\ V_{Y+} \\ V_{Y-} \\ V_{Z+} \\ V_{Z-} \end{pmatrix} \quad (1)$$

Note that DT can be simply applied as SISO (Single-Input Single-Output) OTA. DISO (Differential Input Single Output) OTA implementation requires an additional voltage buffer in order to provide high-impedance inverting input. The implementation of DVCCII by DISO (Differential Input Single Output) OTA and Current Conveyor second generation CCII is shown in Fig. 2.

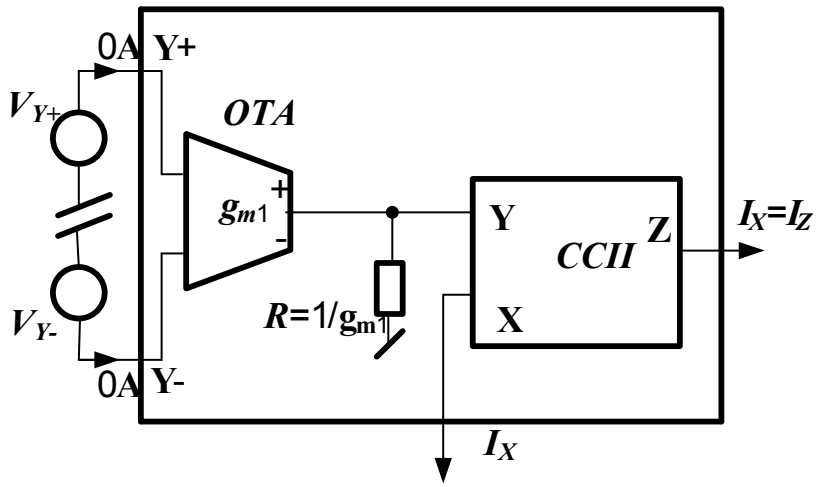

Fig. 2: Implementation of DVCII+ by current conveyor and by OTA.

3. DVCC CMOS CIRCUIT REALIZATION

A. Circuit Description

Fig. 3 shows the circuit realization of the proposed CMOS DVCC of circuit idea in Fig. 2 is based on equalizing the output current of a wide linear range operational transconductance amplifier OTA, formed by transistors (M1-M18). In addition, (M19-M29) comprise a current conveyor second generation CCII. The aspect ratios of each of the transistors used the CCII in Fig. 3 are listed in Table1.

V_{DD}& V_{SS} = ±0.6V, R_{bias} = R_{1bias}= 5kΩ, R_C = R_{C1}=R_{C2} = 4.7kΩ, C_C = C_{C1}= C_{C2}=0.5pF

Transistor	Length (µm)	Width (µm)
M_1,M_2, M_{12},M_{13},M_{19},M_{20}	2	30
M_3,M_4, M_{14},M_{15},M_{21},M_{22}	2	4
M_5,M_{10}, M_{16}, M_{23}, M_{28}	3	20
M_6,M_8, M_{17},M_{24},M_{26}	2	16
M_7,M_9, M_{18},M_{25},M_{27}	3	40
M_{11},M_{29}	3	10

Table 1. Aspect ratios of the transistors used in the DVCC in Fig. 3.

B. Simulation Results

The performance of the proposed COMS DVCC was verified by performing PSPICE simulations with supply voltages ±0.6 V using 0.18µm TSMC CMOS technology. Simulations were carried out using balanced input voltages. Fig. 4 gives the X and Z voltages versus the differential input voltage, when the proposed DVCC is used to realize a unity gain amplifier. The circuit shows good linearity for differential input voltages between ±0.4V, with total standby power dissipation less than 206µW.

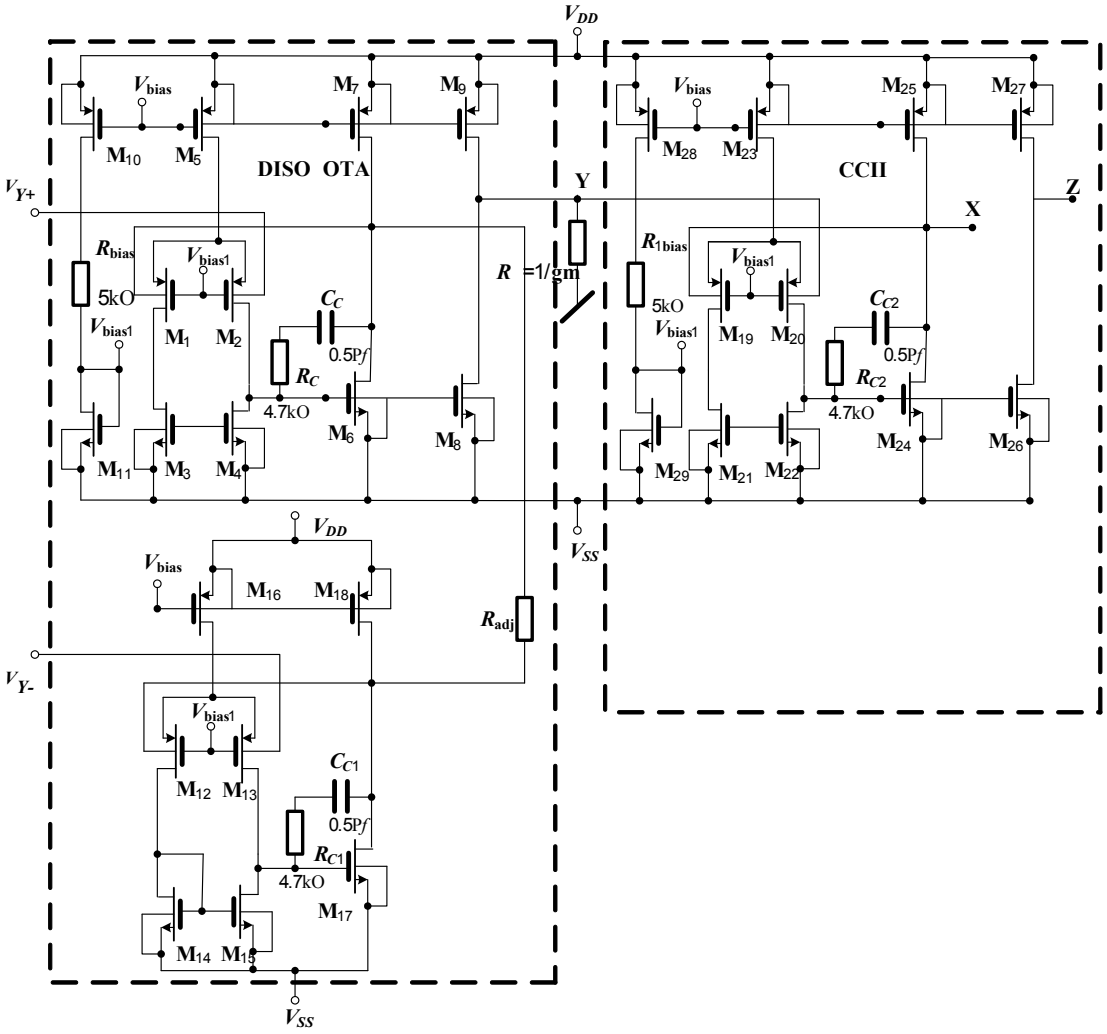

Fig. 3: CMOS Implementation of DVCII+ by Bulk-driven current conveyor and by OTA.

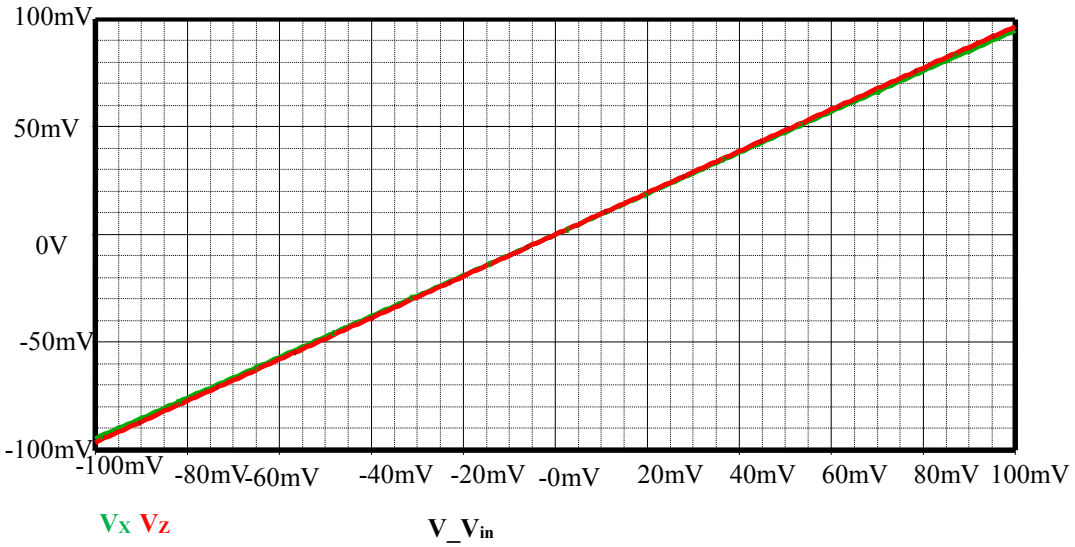

Fig. 4:

The X and Z terminal output voltage versus changes of Vid

4. NEW MULTIIPLE INPUT SINGLE OUTPUT FILTER BASED ON DVCC

In this section the proposed DVCC is used to realize a new multiple input single output second-order LP-BP filter Fig. 5.

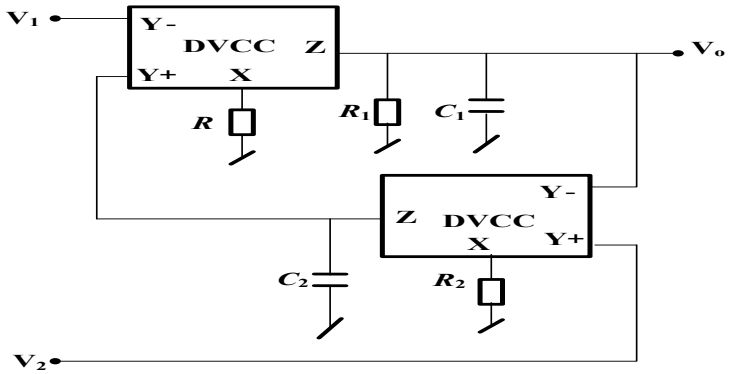

Fig. 5: Block representation of the multiple input single output filter

The transfer function of the filter is depending on the actual active input. Hence, if the first input is active, while the second one is grounded, an inverting BP response is obtained. On the other hand, grounding the first input while activating the second one generates a non inverting LP response. This can be verified through direct analysis, obtaining the following equations:

$$\frac{V_o}{V_1} = -\frac{S/C_1R}{D(S)} \tag{2}$$

$$\frac{V_o}{V_2} = -\frac{1/C_1C_2R_2R}{D(S)} \tag{3}$$

Where

$$D(S) = S^2 + S/C_1R_1 + 1/C_1C_2R_2R_1 \tag{4}$$

$$A_v \text{ Band pass} = -\frac{R_1}{R} \qquad A_v \text{ Low pass} = 1 \tag{5}$$

From equation (4), ω_0 and Q of the filter are given by:

$$\omega_0 = \sqrt{1/C_1C_2R_2R} \tag{6}$$

$$Q = R_1\sqrt{C_1/C_2R_2R} \tag{7}$$

Simulation results prove the aforementioned relations with passive element values given in table 1. In Fig. 6 a LP response is generated by grounding V_1 and applying an ac-varying signal at V_2. The cutoff frequency is equal to 788 kHz, which is very close to the theoretical value. Next, the BP response is tested by grounding V_2 and injecting the ac-varying signal at V_1. The passive elements values were optimized as shown in table II to achieve a BP response with Q =8.20 and f_o = 620 kHz [Fig. 7].

LP Filter	Value	BP Filter	Value
R, R_1, R_2	1.5 KΩ	R, R_1, R_2	2 KΩ, 0.65 KΩ, 0.5KΩ
C_1	0.40 nF	$\boldsymbol{C_1}$	0.9 nF
C_2	0.65 nF	$\boldsymbol{C_2}$	0.3 nF

Table. 2: Passive elements of the filter in Fig. 5.

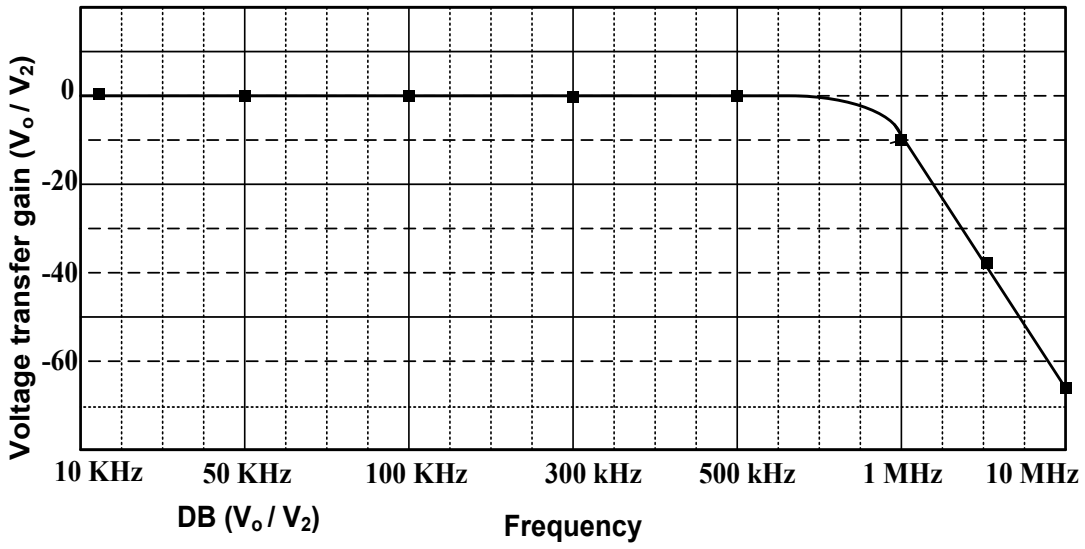

Fig. 6: Low - pass frequency response of the filter

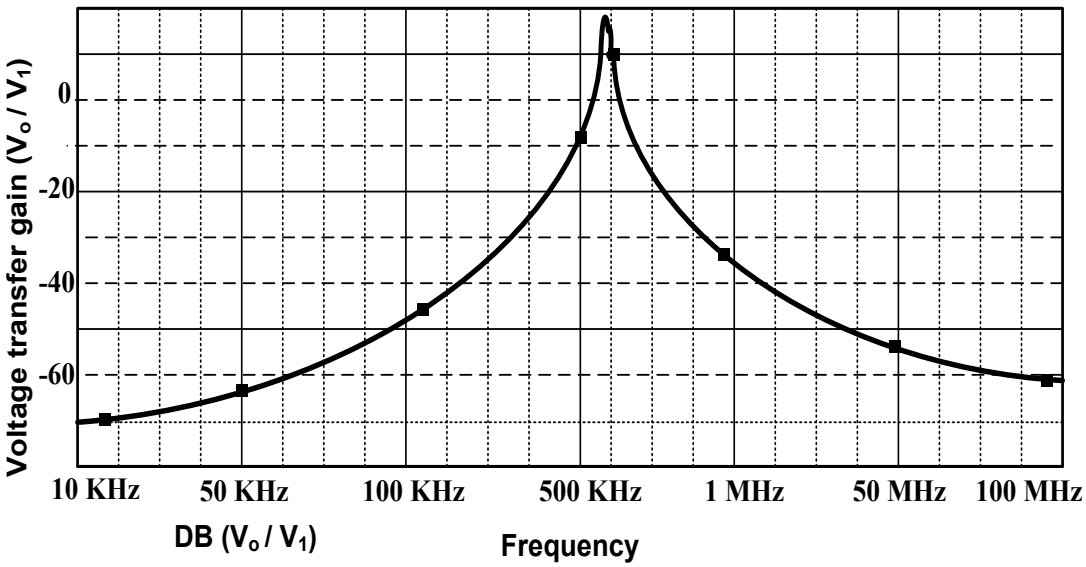

Fig. 7: Band - pass frequency response of the filter

5. CONCLUSION

In this paper, a new wide range CMOS DVCC based on a wide linear range transconductance has been presented. The DVCC has demonstrated a wide dynamic range in the vicinity of ±0.4V for the voltage follower and a ±1mA for the current follower. The

DVCC was used to implement a multiple input single output LP-BP filter. The proposed DVCC circuit and the realized filter have been verified using PSPICE simulations.

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